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Static-Noise-Margin Analysis of Modified 6T SRAM Cell during Read Operation

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***Abstract*—As modern technology is spreading fast, it is very important to design low power, high performance, fast responding SRAM(Static Random Access Memory) since they are critical component in high performance processors. In this paper we discuss about the noise effect of different SRAM circuits during read operation which hinders the stability of the SRAM cell. This paper also represents a modified 6T SRAM cell which increases the cell stability without increasing transistor count**.

***Index Terms*—CMOS logic, Static Noise Margin (SNM), power consumption, SRAM and VLSI.**

I. Introduction

The SRAM sizing has been scaled down due to the increase density of SRAM in System-On-Chip (SoC) and other integrated devices, which works on lower supply voltage. This leads to considerable amount of power saving, but the stability and performance of the SRAM circuit is also being affected due to the scaling of supply voltage. The lower supply voltage reduces the Static Noise Margin on which the stability of the SRAM cell depends. With lower VDD, the delay of SRAM cell increases considerably and thus speed of the SRAM will be lowered. The conventional 6T SRAM cell has the lowest stability, so to remove this problem many new circuitry having larger transistor count i.e. 8T, 9T etc. have been implemented. These circuits are used to increase the cell stability due to increased Static Noise Margin.

II. Conventional 6T Sram

The conventional 6T memory cell comprised of two CMOS invertors cross coupled with two pass transistors connected to a complimentary bit lines as shown in Fig. 1. The gate of access transistors N3 and N4 are connected to the WL (word line) to have data written to the memory cell or read from the memory cell through the BL or BLB(bit lines) during write and read operation. The bit lines act as I/O buses which carry the data from the memory cell to the sense amplifier. SRAM cell perform three different operations, read, write and hold. The stability of SRAM circuit depends on the Static Noise Margin which can be calculated as follows.

III. Static Noise Margin

A basic SNM is obtained by drawing and mirrorring the invertor characteristics and finding the maximum possible square between them. Ref. [2]. This is a graphical technique of estimating the SNM.

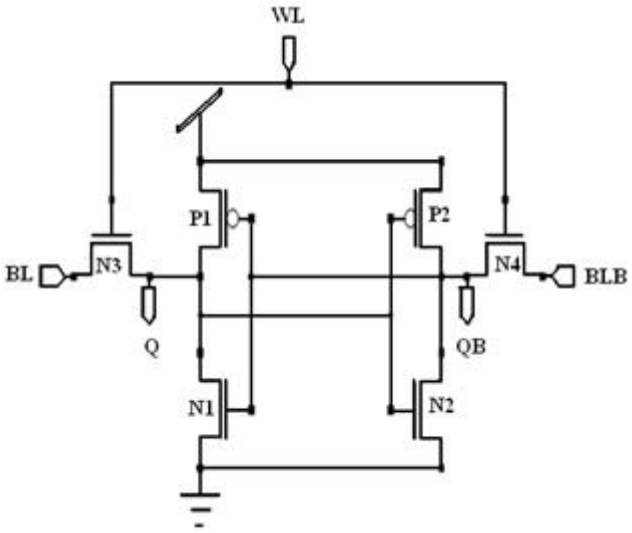

Figure 1. Conventional 6T SRAM Cell

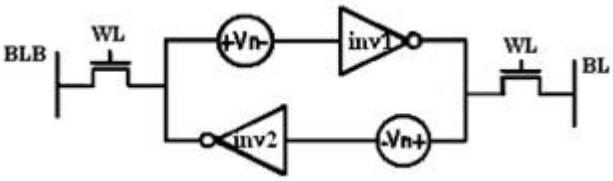

Figure 2. The standard setup for SNM definition [2]

Fig. 2 shows a common way of representing the SNM graphically for a bit-cell holding data.The resulting two-lobed curve is called as a "butterfly curve" as shown in Fig. 3 and is used to determine the SNM.Values of SNM varry in different operation mode. SNM is becoming important factor to check the stability during read operation.Its visible in the Fig. 3 that during read operation, the SNM takes its lowest value and the cell is in its weakest state. The SRAM cell immunity to static noise is measured in terms of SNM that quantifies the maximum amount of voltage noise that can be tolerated at the cross-inverters output nodes without flipping the cell Ref. [4]. Any change in the noise, changes the value of the SNM during cell operation. Though the SNM is important during hold, cell stability during active operation represents a more significant limitation to SRAM operation.

The SNM is calculated when the word line is set high and both bit line are still precharged high. Ref. [8]. At the onset of a read access, the access transistor(WL) is set to "1" and the bit-lines are already precharged to "1".The internal node of the bit-cell representing a zero gets pulled upward through the access transistor due to the voltage dividing effect across the access transistor and drive transistor. This increase in

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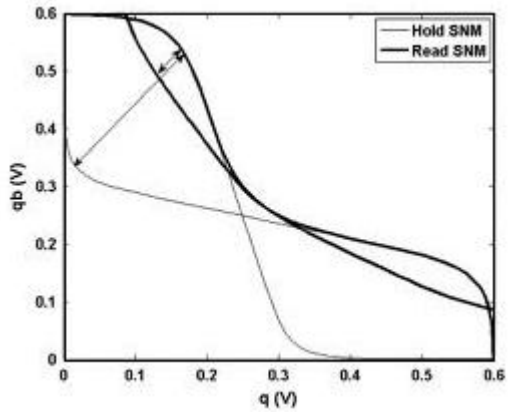

Figure.3 General SNM characteristics during Standby and Read operation

voltage severely degrades the SNM during the read operation as shown in the Fig. 3.

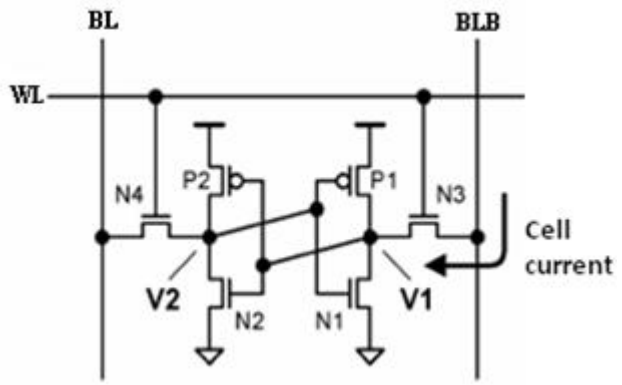

Figure 4. Voltage Stability Problem of 6T SRAM Cell [3]

The 6T SRAM cell has the advantage of low static power dissipation Ref. [3]. However the main reason for the potential instability of this design is such that during the read operation, a stored "0" can be overwritten by a "1" when the voltage at node V1 reaches the V_{th} of NMOS N2 to pull node V2 down to "0"and in turn pull node V1 up even further to "1" due to the mechanism of positive feedback as shown in Fig. 4.

To remove this stability problem many SRAM cell topologies have been implemented which works on the improvement of the stability of the SRAM cell by improving the SNM. These are discussed below.

IV. SRAM TOPOLOGIES

We analyze the performance of various topologies of SRAM Cell for enhancing the cell stability which is related to cell Read-SNM and leakage power consumption.

A. 8T SRAM Cell

To overcome the problem of data storage destruction during read operation, a dual-port 8T-SRAM cell is created by adding two data output transistors to a conventional 6T-SRAM cell as shown in Fig. 5 for which separate read/write bit and word signal lines are used to separate the data retention element and the output element. Ref. [7] In turn the cell implementation provides a read-disturb-free operation. This cell uses eight transistors, which results in cell area

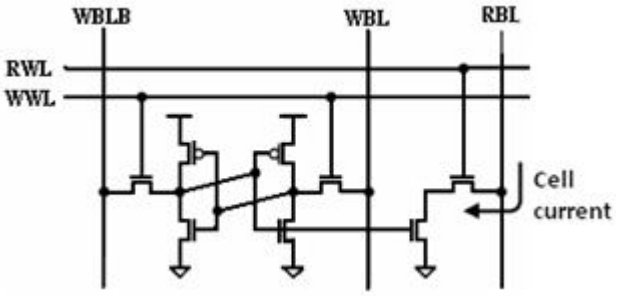

Figure 5. 8T SRAM Cell [3]

increase of 30% in comparison to the conventional 6T-cell design.

By doing this the worse-case stability condition encountered previously in a 6T SRAM cell, is avoided and high read stability is retained.

B. 8T-1 SRAM Cell

Another 8T SRAM Cell Ref. [1] being proposed to reduce the power leakage and improves the SNM. It consists of 8 transistors N1-N5 and P1-P3, as shown in Fig 6. P3 and N5 form an inverter to control the voltage of node C1. The source terminal of P3 is connected to a column select (CS) line while the gates of P3 and N3 are connected to the WL.

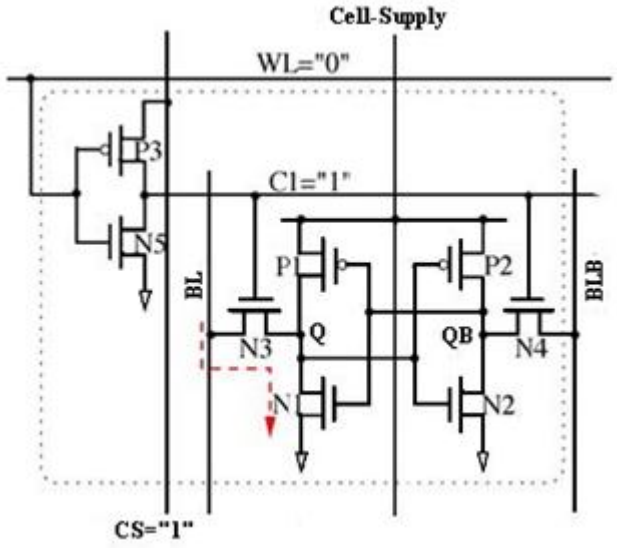

Figure 6. 8T-1 SRAM Cell [1]

As a result N4 and N3 are turned on if and only if both the WL and the CS are triggered. Unlike the conventional design, the sources of P1 and P2 are connected to a dynamic cell supply (*cell-supply*) line which is raised to the higher voltage during the read operation to obtain a higher noise margin. If β=2 for 6T cell design then the area overhead is 33%.The proposed design raises cell supply to 1.5Vdd and hence its SNM is significantly improved.

C. 9T SRAM Cell

A 9T structure is proposed in Ref. [5] to reduce the power consumption of the SRAM cell and the bitline leakage. Fig. 7 shows the proposed 9T SRAM cell. Similarly to the 8T cell , the configuration from M1 to M6 is unchanged (same as in the 6TSRAM cell). The read access is maintained by retaining

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the circuit and adding a NMOS transistor (M9) between M7 and M8. As shown in Fig 7, the leakage current through M7,M8, and M9 can be reduced significantly by the so-called "stack-effect" when M7 and M9 are off.

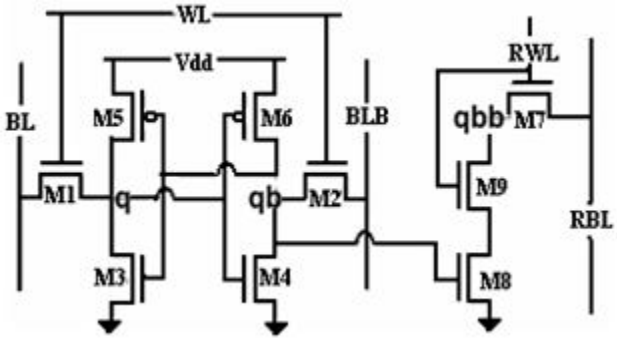

Figure 7. 9T SRAM Cell [5]

The basic idea behind this approach for reduction of leakage power is the effective stacking of transistors in the path from supply voltage to ground. This is based on the observation that "a state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a state with only one transistor OFF in any supply to ground path".

V. Cell Performance Based On Read-Snm

Cell performance of above discussed SRAM cells have been compared with the conventional 6T SRAM cell. All the simulations are based on 45nm technology on Tanner EDA Tool version 13.0, the power supply ranging from 0.4v-1v.The stability of all the SRAM cell is compared by comparing their Read-SNM as shown in Fig 8.

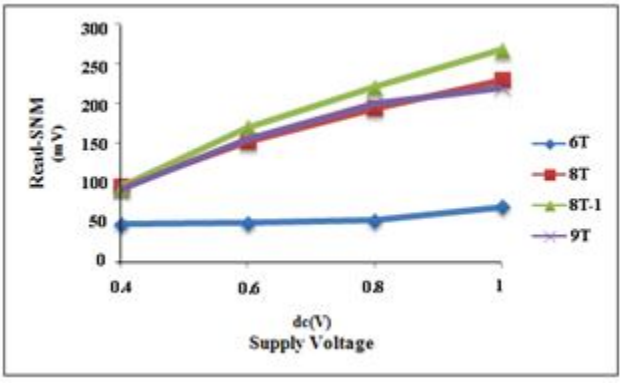

Figure 8. Read SNM verses Power supply voltage of various SRAM topologies

Fig. 8 summarizes the Read-SNM of the four designs in consideration against variation from 1V to 0.4V. As the supply voltage decreases, the read-SNM reduces considerably. It is apparent that the 8T-1 has the highest Read-SNM and the conventional 6T SRAM cell has the lowest Read-SNM, which means it is least stable during read state.

VI. Modified 6T

Recent published works have shown that the Conventional 6T SRAM suffers severe stability degradation due to access disturbance at low–power mode. The conventional 6T SRAM cell has the lowest Read-SNM and thus has lowest stability. So to improve stability of the Conventional 6T SRAM, Read-SNM of the circuit should be improved, so to remove this problem many new circuitry having larger transistor count i.e. 8T, 9T etc. have been implemented. But as we increase the transistor count, read delay and speed for the cell to response, are degraded because of the additional NMOS transistor. Power consumption increases and the probability of switching activity factor rises as the number of transistor increases and those circuits consume larger space. Due to the need of battery operated device, the CMOS technology scaling continues, so there is a modification of Conventional 6T SRAM cell to attain the optimum cell stability by modifying the transistor sizing. The cell stability can also be improved by modifying the Bit-line, Word-line and power supply voltage. The effect of these device parameters show a drastic change in the static noise margin curve of Conventional 6T SRAM Cell.

A. Power-Supply Voltage Modulation Effect

The effect of power supply modulation is important parameter which changes the cell stability during read mode and has been widely acceptable in 45 nm technologies. It is preferable that the supply voltage must be maximum for increase SNM and also cell stability Ref. [6].

Table I. SNM Read Verses Power Supply Voltage Of Modified 6T Sram Cell

Technology (nm)	Power Supply Voltage dc(V)	SNM READ (mV)
45nm	1.0	210
	0.8	189
	0.6	140
	0.4	94

Table I. shows the impact of power supply reduction during Read mode on SNM. It is clear that power supply voltage reduction during read operation is not suitable and SNM is reduced for all cases.

B. Transistor width Modulation Effect

Static Noise Margin of the 6T SRAM cell is affected by the cell ratio(CR) and pull-up ratio(PR).The proper sizing of Driver transistor is responsible for a drastic change in the value of SNM Ref. [9].

Cell ratio is defined as ratio between the sizes of the driver transistor to the size of access transistor (1).

$$CR(\alpha) = \frac{\text{Size of pull down transistor}}{\text{Size of access transistor}} \quad (1)$$

Pull up ratio is nothing but a ratio between sizes of the load transistor to the access transistor (2).

$$PR(\beta) = \frac{\text{Size of pull up transistor}}{\text{Size of access transistor}} \quad (2)$$

To keep cell area within reasonable values, we restrict the values of α and β ratios between the minimum, 1, and a maximum of 2.5, (i.e. $\alpha max = \beta max = 2.5$).

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TABLE II. CELL RATIO VERSES SNM READ

Technology (nm)	CR(α)	SNM READ (mV)
45nm	1.0	70
	1.5	131
	2.0	150
	2.5	161

The SNM gain shows a considerable amount of change while changing the cell ratio as shown in Table II. The SNM increases when increasing the α ratio but when increasing both α and β ratio, provides a higher SNM improvement as shown in Table III.

TABLE III. IMPROVED SNM READ BY VARYING BOTH CELL RATIO AND PULL-UP RATIO

CR(α)	PR(β)	SNM READ (mV)
1.0	1.0	70
1.0	2.0	80
2.0	1.0	150
2.5	1.5	190
2.5	2.5	210

C.Word-Line Modulation Effect

The SRAM cell stability can also be increased with the help of word line voltage modulation for low power supply. This approach is based on reducing the maximum voltage swing of the word-line to maintain the cell during read operation. Fig. 9 plots the relationship between the SNM and the word-line voltage.

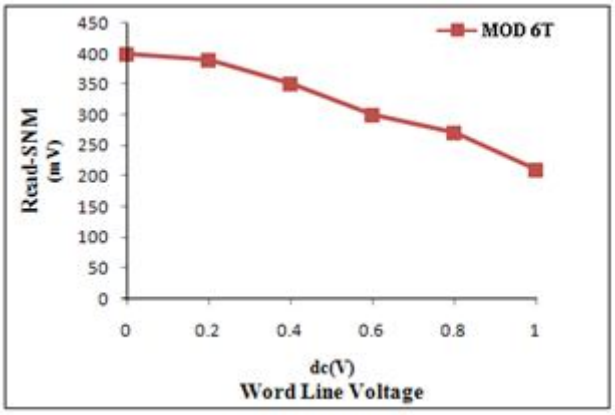

Figure 9. Effect on SNM Read by modulating Word-line Voltage

Reducing the effective word-line voltage could provide an interesting technique to improve the stability of the cell during read operations. As we approach to zero Word-line voltage, the SNM is maximum. The reason behind maximum SNM is that, at WL="0", the SRAM is in standby mode and static noise margin is maximum at hold operation as already seen in Fig. 3.

D. Bit-Line Modulation Effect

The SNM can be improved by increasing the bit-line voltage during read operations. Bit line voltage effectively changes the value of SRAM. Fig. 10 shows the graph between the Read-SNM and the Bit line voltage. As the Bit line voltage increases, the value of SNM also increases. This technique increases the cell stability and is suitable for voltage modulation.

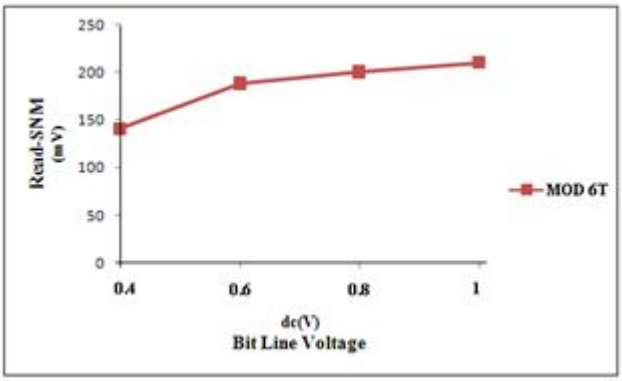

Figure 10. Effect on SNM Read by modulating Bit-line voltage

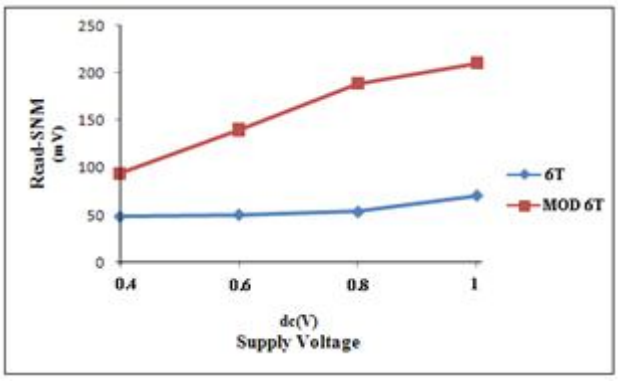

Figure 11. SNM Read Comparisons of conventional 6T and Modified 6T SRAM at different Supply Voltage

Fig. 11 shows the overall comparison of conventional 6T SRAM cell verses Modified 6T SRAM cell by varying power supply voltage. Thus by modifying conventional 6T SRAM cell, the Read-SNM can be improved to a greater extent.

CONCLUSION

The simulation results of all these parameters discussed above improve the read-mode SNM of Modified 6T SRAM. The higher SNM can be achieved by modifying the conventional 6T SRAM cell without requiring any modification of the SRAM cell array design. So to overcome the SNM problem encountered with conventional 6T SRAM cell and to avoid the area overhead occurred due to additional transistors, we have developed an improved Read-SNM by the Modified 6T SRAM Cell.

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